high load current without allowing VCCI to fall below acceptable levels.

The voltage at which the output of comparator **100** switches is referred to as the "trip-point". The trip-point is centered at VREF as shown in FIG. **4**. The hysteresis voltage (indicated by ΔV in FIG. **4**) is selected by the size of transistors **304** and **314** which is determined when comparator **101** is designed to meet the needs of a particular application. Wider transistors result in a larger hysteresis voltage. In the particular example both transistor **304** and **314** are similarly sized to provide symmetric hysteresis. However, the transistors can have different sizes to provide asymmetric hysteresis if desired. Alternatively, transistor **304** can be implemented by a plurality of parallel coupled transistors that can be individually programmably coupled to the VREF signal by, for example, mask programmable or field programmable techniques. This latter technique allows the hysteresis voltage to be programmed. The benefits of the present invention are greatly exploited in hysteretic DC-DC converters where the accuracy and speed of the comparator are important.

FIG. **5** shows a specific CMOS implementation of hysteresis timing unit **102** in accordance with the present invention. In the particular example, VHYST+ is derived directly from the VDCPRE signal described hereinbefore. In the preferred implementation, VDCPRE is an internal control signal that operates on VCCI voltage levels. To ensure that transistor **313** shown in FIG. **1** is turned on fully, it is desirable to shift the VDCPRE signal to a logic level driven from VCCEXT. Any available voltage shift technique may be used to implement voltage shift unit **502**. Care should be exercised in implementing voltage shift unit **502** to ensure that any delays associated with voltage shift unit **502** are acceptable (i.e., allow VHYST+ to react quickly enough to turn on transistor **313** when VDCPRE indicates that a high current load is being activated).

Likewise, NOR gate **503** should be driven from VCCEXT to ensure full turn on of transistor **303** shown in FIG. **3**. The signal on node **105** is logically combined with the voltage translated output of voltage shift unit **502** by NOR gate **503** to generate the VHYST− signal. Again, care should be taken to ensure that any delays associated with NOR gate **502** provide acceptable timing margin for the turn on of transistor **303** when VDCPRE indicates that a high current load is being turned off.

FIG. **6** (prior art) and FIG. **7** show waveforms illustrating the improved performance of the voltage down converter in accordance with the present invention. Just after time **00** comparator **101** is enabled by the VDCENB signal. Because VTRIM is slightly greater than VREF at this time, VDRIVE falls to prevent driver **103** from turning on. At about time **10** a high current load is activated and VCCI begins to drop along with VTRIM that follows VCCI. When VTRIM falls below VREF the VDRIVE signal turns on. However, by the time driver **103** is turned on, VCCI has already experienced significant droop which is worst during from about time **15** to about time **30**. Driver **103** continues to supply charge to filter capacitor **106** until VTRIM rises above VREF at about time **40**. However, by time **40** VCCI has already experienced an overshoot because the high current load was turned off. Once the load is off, VCCI can remain in an overvoltage state for some time because little load current is required and so filter capacitor **106** remains charged.

In contrast, FIG. **7** shows a similar high load switching situation handled by the voltage down converter in accordance with the present invention. In this case, the high current load turn on is anticipated by the VDCPRE signal which goes high just after time **00**. VHYST+ goes high simultaneously to the VCCEXT level while VHYST− remains low. After VHYST+ goes high VDRIVE goes high at about time **05** before a voltage droop on VCCI is apparent. This action is in contrast to the prior art shown in FIG. **6**, where VDRIVE could not respond until after VCCI began to droop.

As VDCPRE and VHYST+ fall just after time **15**, VHYST− goes high to turn on transistor **303** shown in FIG. **3**. Again, the VHYST− timing is selected to anticipate the voltage overshoot condition that occurs when the high current load is turned off. In response to VHYST− going high and VTRIM rising to a voltage just below VREF, VDRIVE falls just before time **20** thereby turning off driver **103**. As a result, the VCCI waveform is markedly flatter and consistently near to the target VCCI specification throughout the high load current switching event using the method and apparatus in accordance with the present invention.

Although the invention has been described and illustrated with a certain degree of particularity, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the combination and arrangement of parts can be resorted to by those skilled in the art without departing from the spirit and scope of the invention, as hereinafter claimed.

I claim:

1. A voltage down converter comprising:

an input node receiving an external voltage VEXT;

a driver unit selectively coupling the input node to an internal voltage supply node in response to a drive control signal;

a reference voltage generator providing a voltage VREF;

a hysteresis timing unit responsive to a first control signal and generating one or more control signals selected from the group consisting of a second control signal VHYST− and a third control signal VHYST+; and

a comparator unit coupled to the internal voltage supply node, VREF, VHYST− and VHYST+ and coupled to the driver unit to generate the drive control signal, the comparator unit shifting a trip point of the comparator in response to the second and third control signals.

2. The voltage down converter of claim **1** wherein the comparator unit further comprises:

a differential input stage having a first input coupled to a signal that is proportional to the voltage on the internal voltage supply node, a second input coupled to VHYST−, a third input coupled to VREF, and a fourth input coupled to VHYST+, and an output, wherein the input stage generates the drive control signal.

3. The voltage down converter of claim **2** wherein the differential input stage comprises:

a first branch within the differential input stage comprising a first load device, a primary current path providing a current through the first load device that is proportional to the voltage on the internal voltage supply node, and supplementary current path providing a current through the first load device when the VHYST− signal is active; and

a second branch within the differential input stage comprising a second load device, a primary current path providing a current through the second load device that is responsive to the reference voltage, and supplementary current path providing a current through the second load device when the VHYST+ signal is active.

4. The voltage down converter of claim 3 wherein the primary current path of the first branch comprises a first field effect transistor coupled in series with the first load device having a gate electrode coupled to a signal that is proportional to the voltage on the internal voltage supply node; and

wherein the supplementary current path of the first branch comprises a second and a third field effect transistor coupled in series with each other and with the first load device, wherein the gate of the second field effect transistor is coupled to the VHYST− signal and the gate of the third field effect transistor is coupled to the reference voltage generator.

5. The voltage down converter of claim 3 wherein the primary current path of the second branch comprises a first field effect transistor coupled in series with the second load device having a gate electrode coupled to the reference voltage generator; and

wherein the supplementary branch of the second current path comprises a second and a third field effect transistor coupled in series with each other and with the second load device, wherein the gate of the second field effect transistor is coupled to the VHYST+ signal and the gate of the third field effect transistor is coupled to the reference voltage generator.

6. The voltage down converter of claim 1 wherein the hysteresis timing unit further comprises:

a first input coupled to the drive control signal;

a second input coupled to receive a clock signal, wherein the clock signal is selected to anticipate activation and deactivation of a high current load coupled to the internal voltage supply node; and

a logic circuit for combining signals on the first and second inputs to generate the first control signal VHYST−.

7. The voltage down converter of claim 6 wherein the hysteresis timing unit further comprises:

a voltage shift circuit coupled to the second input to shift the signal on the second input from a logic level based on the internal supply voltage to a logic level compatible with the external voltage.

8. A method for converting voltage VCC supplied to a pin of an integrated circuit to a lower internal voltage VCCI on an internal voltage supply node, the method comprising the steps of:

generating a first signal proportional to the internal voltage;

coupling the first signal to a comparator, the comparator operating to generate a second signal indicating when the first signal is above or below the trip point;

monitoring a clock signal to anticipate current load in the integrated circuit; and

shifting the trip point in response to the clock signal.

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